

**AMENDMENTS TO THE SPECIFICATION**

Please REPLACE paragraph 0008 on page 3, lines 1-17, with the following:

As shown in FIG. 1A, a metal material is deposited onto a transparent substrate 10 and then patterned to form a gate line, a gate electrode 12 and a gate pad 14. The gate electrode 12 may include a lower layer 12A and an upper layer 12B. The gate pad 14 may include a lower layer 14A and an upper layer 14B. As shown in FIG. 1B, a gate insulating film 16 is formed at the upper portion of the transparent substrate 10 provided with the gate line, the gate electrode 12 and the gate pad 14. Thereafter, an amorphous silicon layer and an amorphous silicon layer doped with an impurity are sequentially formed and then patterned, to thereby form an active layer 18 and an ohmic contact layer 20. As shown in FIG. 1C, a metal material is deposited onto the upper portion of the gate insulating film 16 provided with the active layer 18 and the ohmic contact layer 20 and then patterned, to form source and drain electrodes 22 and 24, a data line and a data pad. The source and drain electrodes 22 and 24 may include lower layers 22A and 24A and upper layers 22B and 24B Subsequently, the ohmic contact layer 20 exposed between the source electrode 22 and the drain electrode 24 is etched to expose the active layer 18. As shown in FIG. 1D, an insulating material is entirely deposited onto the substrate having such a structure to form a protective film 26 and then is patterned, to thereby define a contact hole for exposing the drain electrode 24 and a contact hole for exposing the gate pad 14 and the data pad. As shown in FIG. 1E, a transparent electrode material is entirely deposited thereon and then patterned, to thereby form a pixel electrode 28 contacting the drain electrode 24 and a protective electrode 30 contacting the gate pad 14 and the data pad.